CLAIMS

What is claimed is:

1. A method of fabricating MOSFET transistors in a semiconductor device, comprising:

implanting a first transistor region associated with a first transistor device in the semiconductor device using a first implantation process to adjust a threshold voltage associated with the first transistor device;

implanting a portion of a second transistor region associated with a second transistor device in the semiconductor device to form a source/drain region associated with the second transistor device using the first implantation process;

forming a first gate oxide structure overlying a channel region in the first transistor region, the first gate oxide structure having a first thickness; and

forming a second gate oxide structure overlying a channel region in the second transistor region, the second gate oxide structure having a second thickness, the second thickness being greater than the first thickness.

2. The method of claim 1, further comprising implanting a portion of the first transistor region to form a source/drain region associated with the first transistor device using a second implantation process.

3. The method of claim 2, further comprising:

implanting a third transistor region associated with a third transistor device in the semiconductor device using a third implantation process to adjust a threshold voltage associated with the third transistor device;

implanting a portion of a fourth transistor region associated with a fourth transistor device in the semiconductor device to form a source/drain region associated with the fourth transistor device using the third implantation process;

forming a third gate oxide structure overlying a channel region in the third transistor region, the third gate oxide structure having a third thickness; and

forming a fourth gate oxide structure overlying a channel region in the fourth transistor region, the fourth gate oxide structure having a fourth thickness, the fourth thickness being greater than the third thickness.

4. The method of claim 3, further comprising implanting a portion of the third transistor region to form a source/drain region associated with the third transistor device using a fourth implantation process.

5. The method of claim 3, wherein the first and third transistor devices comprise a first one of an NMOS transistor and a PMOS transistor, and wherein the second and fourth transistor devices comprise a second one of an NMOS transistor and a PMOS transistor.

6. The method of claim 3, wherein the first and third transistor devices comprise NMOS transistors, wherein the second and fourth transistor devices comprise PMOS transistors, and wherein implanting the third transistor region and a portion of the fourth transistor region using the third implantation process comprises implanting phosphorus in the third transistor region and a portion of the fourth transistor region.

7. The method of claim 6, wherein implanting phosphorus in the third transistor region and a portion of the fourth transistor region comprises:

performing a phosphorus threshold adjustment implantation in the third transistor region and a portion of the fourth transistor region [illegible] about 8 E11 cm^{-2} and an energy of about 20 keV; and

performing a phosphorus punch-through implantation in the third transistor region and a portion of the fourth transistor region using a dose of about 2 E12 cm^{-2} and an energy of about 70 keV.

8. The method of claim 4, wherein the first and third transistor devices comprise NMOS transistors, wherein the second and fourth transistor devices

comprise PMOS transistors, and wherein implanting a portion of the third transistor region using the fourth implantation process comprises implanting boron in a portion of the fourth transistor region.

9. The method of claim 8, wherein implanting boron in a portion of the fourth transistor region comprises performing a boron LDD implantation in a portion of the fourth transistor region using a dose of about 4 E13 cm^{-2} and an energy of about 20 keV.

10. The method of claim 2, wherein the first transistor device comprises an NMOS transistor, wherein the second transistor device comprises a PMOS transistor, and wherein implanting a portion of the first transistor region using the second implantation process comprises implanting at least one of phosphorus and arsenic in a portion of the first transistor region.

11. The method of claim 10, wherein implanting at least one of phosphorus and arsenic in a portion of the first transistor region comprises performing a phosphorus LDD implantation in a portion of the first transistor region using a dose of about 4 E13 cm^{-2} and an energy of about 40 keV.

12. The method of claim 1, wherein the first transistor device comprises an NMOS transistor, wherein the second transistor device comprises a PMOS

second transistor region using the first implantation process comprises implanting boron in the first transistor region and a portion of the second transistor region.

13. The method of claim 12, wherein implanting boron in the first transistor region and a portion of the second transistor region comprises:

performing a boron threshold adjustment implantation in the first transistor region and a portion of the second transistor region using a dose of about 3 E12 cm^{-2} and an energy of about 20 keV; and

performing a boron punch-through implantation in the first transistor region and a portion of the second transistor region using a dose of about 4 E12 cm^{-2} and an energy of about 70 keV.

14. The method of claim 1, wherein the first thickness is about 65 Å or more and the second thickness is about 300 Å or less.

15. The method of claim 14, wherein the first thickness is about 75 Å and the second thickness is about 200 Å.

16. The method of claim 1, wherein first transistor device comprises a PMOS transistor, wherein the second transistor device comprises an NMOS transistor, and wherein implanting the first transistor region and a portion of the second transistor region using the first implantation process comprises implanting phosphorus in the first transistor region and a portion of the second transistor region.

17. The method of claim 16, wherein implanting phosphorus in the first transistor region and a portion of the second transistor region comprises:

transistor region and a portion of the second transistor region using a dose of about 8 E11 cm^{-2} and an energy of about 20 keV; and

performing a phosphorus punch-through implantation in the first transistor region and a portion of the second transistor region using a dose of about 2 E12 cm^{-2} and an energy of about 70 keV.

18. A method of fabricating MOSFET transistors in a semiconductor device, comprising:

adjusting a threshold voltage of a first transistor device using a first threshold adjust implantation process; and

forming a source/drain region of a second transistor device using the first threshold adjust implantation process.

19. The method of claim 18, further comprising forming a source/drain region of the first transistor device using a first LDD implantation process.

20. The method of claim 19, further comprising:

forming a first gate oxide structure of the first transistor device having a first thickness; and

forming a second gate oxide structure of the second transistor device having a second thickness, the second thickness being greater than the first thickness.

21. The method of claim 19, further comprising:

adjusting a threshold voltage of a third transistor device using a second threshold adjust implantation process; and

forming a source/drain region of a fourth transistor device using the second threshold adjust implantation process.

22. The method of claim 21, further comprising forming a source/drain

23. The method of claim 22, wherein the first and third transistor devices comprise a first one of NMOS transistors and PMOS transistors, and wherein the second and fourth transistors comprise a second one of NMOS transistors and PMOS transistors.

24. The method of claim 18, wherein the first transistor device comprises an NMOS transistor, wherein the second transistor device comprises

a PMOS transistor, and wherein adjusting a threshold voltage of the first transistor device and forming a source/drain region of the second transistor device using the first threshold adjust implantation process comprises selectively implanting a first transistor region associated with the first transistor device to adjust a threshold voltage associated with the first transistor device, and implanting a portion of a second transistor region associated with the second transistor device to form a source/drain region associated with the second transistor device using boron.

25. The method of claim 18, wherein the first transistor device comprises a PMOS transistor, wherein the second transistor device comprises an NMOS transistor, and wherein adjusting a threshold voltage of the first transistor device and forming a source/drain region of the second transistor device using the first threshold adjust implantation process comprises selectively implanting a first transistor region associated with the first transistor device to adjust a threshold voltage associated with the first transistor device, and implanting a portion of a second transistor region associated with the second transistor device to form a source/drain region associated with the second transistor device using phosphorus.

26. A method of forming a source/drain region in a semiconductor device, comprising:

[illegible] region to adjust a threshold voltage associated with a first transistor device and a portion of a second transistor region to form a source/drain region associated with a second transistor device using a single implantation process.

27. The method of claim 26, wherein selectively implanting the first transistor region and a portion of the second transistor region comprises implanting one of phosphorus, arsenic and boron in the first transistor region and a portion of the second transistor region.

28. A method of fabricating a semiconductor device, comprising:

implanting an active region of a low voltage NMOS device and source/drain regions of a high voltage PMOS device using a boron threshold voltage adjust implantation process;

implanting an active region of a low voltage PMOS device and source/drain regions of a high voltage NMOS device using a phosphorus threshold voltage adjust implantation process;

forming polysilicon gate structures associated with the high and low voltage NMOS and PMOS devices;

implanting source/drain regions associated with the low voltage NMOS device using a phosphorus or arsenic LDD implantation process; and

implanting source/drain regions associated with the low voltage PMOS device using a boron LDD implantation process.

29. The method of claim 28, further comprising:

forming sidewall spacers on opposite sides of the polysilicon gate structures;

further implanting the source/drain regions associated with the low and high voltage NMOS devices using a phosphorus or arsenic implantation process; and

further implanting the source/drain regions associated with the low and

[illegible] implantation process

30. The method of claim 29, further comprising:

forming a first gate oxide layer having a first thickness overlying the active regions associated with the low voltage NMOS and PMOS devices; and

forming a second gate oxide layer having a second thickness overlying the active regions associated with high voltage NMOS and PMOS devices, wherein the second thickness is greater than the first thickness.